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UNITED STATES PATENT APPLICATION

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FOR

ETCH STOP LAYER FOR ETCHING FINFET GATE OVER A LARGE TOPOGRAPHY

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TECHNICAL FIELD

[0001] The present invention relates generally to transistors and, more particularly, to fin field effect transistors (FinFETs).

BACKGROUND ART

[0002] Scaling of device dimensions has been a primary factor driving improvements in integrated circuit performance and reduction in integrated circuit cost. Due to limitations associated with existing gate-oxide thicknesses and source/drain (S/D) junction depths, scaling of existing bulk MOSFET devices below the 0.1 μm process generation may be difficult, if not impossible. New device structures and new materials, thus, are likely to be needed to improve FET performance.

[0003] Double-gate MOSFETs represent new devices that are candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, the use of two gates to control the channel significantly suppresses short-channel effects. A FinFET is one example of a recent double-gate structure that includes a channel formed in a vertical fin. The FinFET is similar to existing planar MOSFETs in layout and fabrication. The FinFET also provides a range of channel lengths, CMOS compatibility and large packing density compared to other double-gate structures.

DISCLOSURE OF THE INVENTION

[0004] Consistent with the present invention, methods for forming a FinFET gate are provided that alleviate problems that occur, using conventional gate formation processes, because of anti-reflective coating (ARC) over-etch due to high topography. During

conventional ARC etching to form a FinFET gate, using, for example, CF_4 or CHF_3 etching processes, the underlying polysilicon gate material can be attacked, thus, increasing the chance of source/drain attack (e.g., rough or dirty fin sidewalls), pitting and poor profile. To alleviate this problem, an etch stop layer may be formed, consistent with the invention, between the ARC and the gate polysilicon. The etch stop layer prevents over-etching of the ARC, that may occur due to the severe topography of the Fin device, from attacking the source/drain regions or gate material of the FinFET. The etch stop layer may include Ti or TiN that has a very low etch rate in a fluorine etching process, such as, for example, a CF_4/Ar etching process. Subsequent to etching of the ARC, the etch stop layer and polysilicon material of the gate may be etched using, for example, a Cl_2/HBr etching process.

[0005] Additional advantages and other features of the invention will be set forth in part in the description which follows and, in part, will become apparent to those having ordinary skill in the art upon examination of the following, or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

[0006] According to the present invention, the foregoing and other advantages are achieved in part by a method of forming a gate for a FinFET. The method includes forming a first layer of material over a fin and forming a second layer over the first layer, the second layer including at least one of Ti and TiN. The method further includes forming a third layer over the second layer, the third layer comprising an anti-reflective coating and etching the first, second and third layers to form the gate for the FinFET.

[0007] According to another aspect of the invention, a method of forming a gate electrode for a FinFET is provided. The method includes forming a first layer over a fin and forming an etch stop layer over the first layer. The method further includes applying an anti-reflective coating to the etch stop layer and forming a photo-resist layer in a gate pattern over the anti-

relective coating. The method also includes etching the anti-reflective coating and etching the etch stop layer and the first layer to form the gate electrode in the first layer in a shape corresponding to the gate pattern.

[0008] According to a further aspect of the invention, a structure for forming a FinFET is provided. The structure includes a fin formed on a substrate and a first layer formed over the fin. The structure further includes a second layer formed over the first layer, the second layer including at least on of Ti and TiN. The structure also includes a third layer formed over the second layer, the third layer including an anti-reflective coating, and wherein the first, second and third layers are etched to form a gate for the FinFET in the first layer.

[0009] Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

[0011] FIGS. 1A and 1B illustrate an exemplary FinFET fin channel and source/drain formed on a substrate consistent with the present invention;

[0012] FIGS. 2A and 2B illustrate an polysilicon layer, etch stop layer, anti-reflective coating, and photo-resist layer formed on the fin channel and source/drain of FIGS. 1A and 1B consistent with the invention;

[0013] FIG. 3 illustrates a cross-sectional view of etching of the anti-reflective coating of FIG. 2A consistent with the invention;

[0014] FIG. 4 illustrates a cross-sectional view of etching of the etch stop layer and polysilicon layer of FIG. 3 consistent with the invention;

[0015] FIGS. 5A and 5B illustrate a gate formed upon the fin channel and source/drain of FIG. 1A consistent with the invention;

[0016] FIG. 6 illustrates a cross-sectional view of an exemplary polysilicon layer formed on the fin channel and source/drain of FIG. 1A consistent with another embodiment of the invention;

[0017] FIG. 7 illustrates a cross-sectional view of an exemplary endpoint layer and spacer formed on the polysilicon layer of FIG. 6 consistent with the invention;

[0018] FIG. 8 illustrates etching of the spacer of FIG. 7 consistent with the invention;

[0019] FIGS. 9A and 9B illustrate an exemplary FinFET fin channel and source/drain formed on a substrate consistent with yet another embodiment of the invention;

[0020] FIG. 10 illustrates a cross-sectional view of an exemplary dielectric and protective layer formed on the fin channel of FIG. 9A consistent with the invention;

[0021] FIG. 11 illustrates a cross-sectional view of an exemplary polysilicon layer formed on the fin channel and source drain of FIGS. 9A and 9B consistent with the invention;

[0022] FIG. 12 illustrates a cross-sectional view of an exemplary bottom anti-reflective coating and photo-resist layer formed on the polysilicon layer of FIG. 11 consistent with the invention;

[0023] FIG. 13 illustrates a cross-sectional view of an exemplary gate formed by etching the bottom anti-reflective coating and polysilicon layer of FIG. 12 consistent with the invention; and

[0024] FIGS. 14A and 14B illustrate removal of bottom anti-reflective coating and photo-resist from the exemplary gate of FIG. 13 consistent with the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0025] The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims.

[0026] Consistent with the present invention, an etch stop layer may be formed between an ARC and a polysilicon layer used to form a FinFET gate. The etch stop layer may prevent over-etching of the ARC, that can occur due to the severe topography of the fin device, from attacking the source/drain regions or gate material of the FinFET. The etch stop layer may include Ti or TiN that has a very low etch rate in a fluorine etching process, such as, for example, a CF_4/Ar etching process.

[0027] FIGS. 1A and 1B illustrate a FinFET fin channel and source/drain (S/D) 105 formed on a buried oxide layer 110 in accordance with an exemplary embodiment of the present invention. Fin channel and S/D 105 may be formed on buried oxide layer 110 using any conventional technique. Fin channel and S/D 105 may include, for example, silicon (Si). Other materials, such as Germanium (Ge), may alternatively be used.

[0028] As shown in FIG. 2A, a layer 205 of polysilicon, for example, may be formed over fin channel and S/D 105. FIG. 2A is a cross-sectional view taken along the line A-A' in FIG. 1B. Polysilicon layer 205 may be formed, for example, using conventional deposition processes. The thickness of polysilicon layer 205 may range, for example, from about 500Å to about 2000Å. After forming polysilicon layer 205, an etch stop layer 210 may be formed on polysilicon layer 205. Etch stop layer 210 may include, for example, Ti or TiN. The thickness of layer 210 may range, for example, from about 50Å to about 150Å. An anti-reflective coating (ARC) 215 may then be applied to etch stop layer 210. ARC 215 may be applied, for example, using existing spin-on or chemical vapor deposition (CVD) techniques. ARC 215 may include,

for example, SiN ARC. As shown in FIGS. 2A and 2B, a photo-resist layer 220, patterned in the shape of a desired FinFET gate, may be formed on ARC 215. Photo-resist layer 220 may include any type of existing photo-resist material employed in conventional photolithography.

[0029] After formation of polysilicon layer 205, etch stop layer 210, ARC 215, and photo-resist layer 220, ARC layer 215 may be etched away, as shown in FIG. 3, using, for example, a CF4/Ar etching process. Since the Ti or TiN of etch stop layer 210 has a very low etch rate in F-based chemistries, owing to the low vapor pressure of TiF_4 type product species at typical polysilicon gate plasma etch temperatures of 50-70 degrees C, a large over etch of ARC 215 can occur without effecting polysilicon layer 205. As shown in FIG. 4, etch stop layer 210 and polysilicon layer 205 may then be etched using, for example, a Cl_2/HBr or $Cl_2/N_2/O_2$ etching process. After etching, any remaining portions of etch stop layer 210, ARC 215 and photo-resist layer 220 may be removed to leave polysilicon layer 205 formed in the shape of gate 505, as shown in FIGS. 5A and 5B.

EXEMPLARY SPACER FOR GATE FORMATION

[0030] When using conventional processes, the severe topography of the FinFET device increases the chances of process errors when forming the FinFET gate. The topography can change the effective coated thickness of photo-resist on fin structures. Since the resist thickness affects the net reflectance and hence the retained dose, critical dimension of the gate features can vary over the wafer. This dimension needs good control to attain proper device performance. Hence, any technique to reduce the steep topography on the fin features would be helpful to the overall fabrication. Consistent with another exemplary embodiment of the invention, a spacer may be formed on a layer of material, from which the gate is to be formed, to create a less severe topography that improves the gate formation process.

[0031] As shown in FIG. 6, a layer 605 of polysilicon, for example, may be formed over a fin channel and source/drain, such as fin channel and S/D 105 shown in FIGS. 1A and 1B.

Polysilicon layer 605 may be formed, for example, using conventional deposition processes. The thickness of polysilicon layer 605 may range, for example, from about 500Å to about 2000Å.

[0032] As shown in FIG. 7, an endpoint layer 705 may then be formed on polysilicon layer 605. Endpoint layer 705 may include, for example, a layer of Ti or SiGe in a thickness ranging, for example, from about 50Å to about 100Å. Endpoint layer 705 may be formed, for example, using conventional deposition processes. A spacer 710 may be formed on endpoint layer 705. Spacer 710 may include, for example, polysilicon. If polysilicon is used, the etch steps used for the standard poly gate structure can continue to be used since all the layers (including endpoint indicator) will etch in poly etch chemistry. If alternate materials such as oxide or nitride are used for the spacer, the poly etch process will have to be modified to clear out this spacer first using processes selective to Si such as C_4F_8/CO/Ar or CHF_3/Ar. The thickness of spacer 710 may range, for example, from about 500Å to about 1500Å.

[0033] As shown in FIG. 8, spacer 710 may then be etched, using an existing etching process, to create an etched spacer 805 that has a more gentle topography. Photo-resist may then be applied more uniformly to the gentle topography than would be the case with the sharp step 610 shown in FIG. 6. This applied photo-resist may then be used to etch polysilicon layer 615 into a desired gate shape (not shown).

EXEMPLARY BARC FOR FORMING FINFET GATE

[0034] In some conventional FinFET gate formation processes, a layer of polysilicon (e.g., 200-1500 Å thickness) is deposited over the FinFET fin, followed by a SiRN BARC (e.g., approximately 200 Å thickness). During subsequent etching of the BARC and polysilicon to form the gate, using, for example, fluorine materials, SiRN "stringers" or extra pattern defects may be formed at the corners of the topography due to over etching. Additionally, in instances of extreme over etching of the BARC and polysilicon, the source and drain regions of the fin

may be attacked, or the protective oxide or gate dielectric formed on surfaces of the fin may be damaged or removed.

[0035] In yet another exemplary embodiment of the invention, a process for forming a FinFET gate is provided that enables very small gate electrode patterning (e.g., 10-40nm) without causing the formation of stringers, or source/drain damage to the FinFET device. In this exemplary embodiment of the invention, organic BARC may be formed over the gate polysilicon and etched with HBr/O_2 chemistry or $He/N_2/O_2$ chemistry. Etching of the organic BARC, thus, does not require harsh fluorine containing materials, thereby, reducing damage to the FinFET fin.

[0036] FIGS. 9A and 9B illustrate a FinFET fin channel and source/drain (S/D) 905 formed on a buried oxide layer 910 in accordance with this exemplary embodiment of the invention. Fin channel and S/D 905 may be formed on buried oxide layer 910 using any conventional technique. Fin channel and S/D 905 may include, for example, silicon (Si). Other materials, such as Germanium (Ge), may alternatively be used.

[0037] As shown in FIG. 10, subsequent to formation of fin channel and S/D 905, a dielectric 1005 including, for example, an oxide material, may then be formed on the sidewalls of fin channel 905. Dielectric 1005 may be formed on the sidewalls of fin channel 905 using existing growth or deposition processes. The thickness of dielectric 1005 may range, for example, from about 10Å to about 50Å. A protective layer 910 may be formed on an upper surface of fin channel 905 using, for example, conventional growth or deposition processes. Protective layer 910 may include, for example, SiO_2. The height h of fin 905 and protective layer 910 may range, for example, from about 100 Å to about 1500 Å. A layer of polysilicon 1105 may then be formed on fin 905, as shown in FIG. 11. Polysilicon layer 1105 may be formed using, for example, conventional deposition processes. The thickness of polysilicon layer 1105 may range, for example, from about 500Å to about 2000Å.

[0038] As shown in FIG. 12, a bottom anti-reflective coating (BARC) 1210 may be formed on polysilicon layer 1105. BARC 1210 may be formed using, for example, a conventional spin-on process. These BARCs are typically made of organic materials – standard BARCs of such type used in the industry are AR19, AR40, 1C1B etc. The organic nature of the material (similar to photoresist) enables etching the BARC in chemistries, such as $N_2/O_2/He$ or $HBr/O_2/Ar$, that attack the polysilicon to a negligible extent, thus allowing significant BARC overetch over the steep fin topography. A layer of photo-resist, patterned in a shape of a desired gate, may then be formed on BARC 1210 using conventional techniques. BARC 1210 and polysilicon layer 1105 may then be etched to form polysilicon layer 1105 as a gate 1305 in the shape of photo-resist 1210, as shown in FIG. 13. BARC 1210 may be etched using, for example, conventional HBr/O_2 or $He/N_2/O_2$ etching processes. Polysilicon layer 1105 may be etched, for example, using a conventional Cl_2/HBr etching process. As shown in FIGS. 14A and 14B, BARC 1205 and photo-resist 1210 may then be removed to form a FinFET 1405.

[0039] In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0040] Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.